WHAT IS CLAIMED IS:

1. An output driver for a semiconductor device, the output driver comprising:

a first pre-driver receiving a first signal so as to output a second signal in which a slew rate is controlled;

a second pre-driver receiving a third signal so as to output a fourth signal in which a slew rate is controlled; and

a pull-up transistor and a pull-down transistor connected in series between a power supply voltage and a ground voltage, wherein the pull-up transistor is turned on and/or off by the second signal, and the pull-down transistor is turned on and/or off by the fourth signal.

2. The output driver as claimed in claim 1, wherein the first pre-driver comprises a CMOS inverter for receiving the first signal, a pulse generating circuit for receiving the first signal to output a pulse signal having a constant width, a first control section for receiving the pulse signal outputted from the pulse generating circuit, and a second control section which is turned on and/or off by a control signal outputted from the first control section, and wherein the second control section is positioned between a power

supply voltage and an output end of the CMOS inverter, the second signal represents an output signal outputted through the output end of the CMOS inverter, the first and the second control section are sequentially enabled by the pulse signal generated from the pulse generating circuit, and the power supply voltage is supplied to the output end when the second control section is enabled.

3. The output driver as claimed in claim 2, wherein the second control section is enabled only while the pulse signal is enabled.

4. The output driver as claimed in claim 2, wherein the first control section comprises at least one resistance component and at least one transistor connected in series between the power supply voltage and the ground voltage, and the transistor of the first control section is turned on to enable the second control section while the pulse signal is enabled.

5. The output driver as claimed in claim 4, wherein the CMOS inverter is positioned between the power supply voltage and the ground voltage, and an NMOS transistor of the CMOS inverter has a PVT (process, voltage, and temperature)

variation property similar to that of the transistor of the first control section.

6. The output driver as claimed in claim 5, wherein the transistor of the first control section is an NMOS transistor and the second control section includes a PMOS transistor.

7. The output driver as claimed in claim 1, wherein the first pre-driver comprises a CMOS inverter for receiving the first signal, a first control section for receiving the first signal, and a second control section which is turned on and/or off by a control signal outputted from the first control section, and wherein the second control section is positioned between a power supply voltage and an output end of the CMOS inverter, the second signal represents an output signal outputted through the output end of the CMOS inverter, the first and the second control section are sequentially enabled when the first signal is enabled, and the power supply voltage is supplied to the output end when the second control section is enabled.

8. The output driver as claimed in claim 7, wherein the first control section comprises at least one resistance component and at least one transistor connected in series

between the power supply voltage and the ground voltage, and the transistor of the first control section is turned on to enable the second control section while the first signal is enabled.

9. The output driver as claimed in claim 1, wherein the second pre-driver comprises a CMOS inverter for receiving the third signal, a pulse generating circuit for receiving the third signal to output a pulse signal having a constant width, a first control section for receiving the pulse signal outputted from the pulse generating circuit, and a second control section which is turned on and/or off by a control signal outputted from the first control section, and wherein the second control section is positioned between an output end of the CMOS inverter and a ground voltage, the fourth signal represents an output signal outputted through the output end of the CMOS inverter, the first and the second control section are sequentially enabled by the pulse signal generated from the pulse generating circuit, and the ground voltage is supplied to the output end when the second control section is enabled.

10. The output driver as claimed in claim 9, wherein the second control section is enabled only while the pulse

signal is enabled.

11. The output driver as claimed in claim 9, wherein the first control section comprises at least one resistance component and at least one transistor connected in series between the power supply voltage and the ground voltage, and the transistor of the first control section is turned on to enable the second control section while the pulse signal is enabled.

12. The output driver as claimed in claim 11, wherein the CMOS inverter is positioned between the power supply voltage and the ground voltage, and a PMOS transistor of the CMOS inverter has a PVT variation property similar to that of the transistor of the first control section.

13. The output driver as claimed in claim 12, wherein the transistor of the first control section is a PMOS transistor and the second control section includes an NMOS transistor.

14. The output driver as claimed in claim 1, wherein the second pre-driver comprises a CMOS inverter for receiving the third signal, a first control section for receiving the

third signal, and a second control section which is turned on and/or off by a control signal outputted from the first control section, and wherein the second control section is positioned between an output end of the CMOS inverter and a ground voltage, the fourth signal represents an output signal outputted through the output end of the CMOS inverter, the first and the second control section are sequentially enabled when the third signal is enabled, and the ground voltage is supplied to the output end when the second control section is enabled.

15. The output driver as claimed in claim 14, wherein the first control section comprises at least one resistance component and at least one transistor connected in series between the power supply voltage and the ground voltage, and the transistor of the first control section is turned on to enable the second control section while the third signal is enabled.

16. The output driver as claimed in claim 1, wherein a first and a second resistance component are connected between the pull-up transistor and the pull-down transistor.